WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a semiconductor substrate including semiconductor devices;

a first wiring layer having an associated thickness being located over the substrate and having interconnect wire embedded therein;

a second wiring layer having an associated thickness being located on the first wiring layer and having interconnect wire embedded therein; and

a capacitor having a first metal-based charge-storage electrode, a second metal-based charge-storage electrode, and a dielectric layer interposed between the charge-storage electrodes, the charge-storage electrodes extending through the thickness of the second wiring layer and at least part of the first wiring layer.

2. The circuit of claim 1, wherein the dielectric layer comprises one of Ta_2O_5, $BaSrTiO_4$, Al_2O_3, ZrO_2, and HfO_2.

3. The circuit of claim 1, wherein

a first region of the substrate includes dynamic random access memory cells;

a second region of the substrate includes logic circuits and is physically separate from the first region; and

the capacitor is located in a portion of the wiring layers located over the first region of the substrate.

4. The circuit of claim 3, wherein the capacitor is a functional portion of one of the random access memory cells.

5. The circuit of claim 1, further comprising:

a third wiring layer being located on the second wiring layer and having metal-based interconnect wire embedded therein, the first charge-storage electrode of the capacitor being in physical contact with a portion of the interconnect wire of the third layer.

6. The circuit of claim 1, further comprising:

a tungsten plug being located between the second charge-storage electrode and a portion of the substrate.

7. The circuit of claim 1, wherein at least one of the wiring layers is a dual damascene wiring layer.

8. The circuit of claim 1, further comprising:

a transistor located on the substrate; and

a metal plug electrically connecting the second charge-storage electrode to one of a source and a drain of the transistor.

9. A process for forming an integrated circuit, comprising:

providing a semiconductor substrate with semiconductor devices;

forming a first wiring layer and a portion of a second wiring layer over the substrate;

opening a window through the first wiring layer and the portion of the second wiring layer; and

forming a capacitor in the window, the capacitor having inner and outer charge-storage electrodes that extend through the first wiring layer and the portion of the second wiring layer.

10. The process of claim 9, wherein the forming a capacitor with inner and outer charge-storage electrodes is based on a single masked anisotropic etch.

11. The process of claim 9, wherein the forming a capacitor further comprises:

depositing material for the outer charge-storage electrode on the window;

depositing a dielectric layer on the outer charge-storage electrode; and

depositing material for the inner charge-storage electrode on the dielectric layer.

12. The process of claim 11, further comprising:

removing the deposited material for one of the charge-storage electrodes to form a gap between a surface of the wiring layer farthest from the substrate and the one of the charge-storage electrodes.

13. The process of claim 11, wherein the deposited dielectric layer has a dielectric constant at least as high as the dielectric constant of one of Ta_2O_5, $BaSrTiO_4$, Al_2O_3, ZrO_2, and HfO_2.

14. The process of claim 11, further comprising:

forming another wiring layer over the capacitor, one of interconnect wire and a metal plug in the another wiring layer making physical contact with one of the charge-storage electrodes.

15. The process of claim 9, further

forming a dielectric layer over the substrate; and

forming a metal plug through the dielectric layer, the metal plug contacting one of the devices; and

wherein the forming a capacitor causes one of the charge-storage electrodes to contact the plug.

16. The process of claim 9, wherein the forming a first wiring layer and a portion of a second wiring layer produces at least two wiring layers.

17. A process for fabricating an integrated circuit with embedded memory cells, comprising:

providing a substrate with semiconductor devices for logic circuits and for DRAM cells in first and second physical regions, respectively;

fabricating a first and at least a portion of a second wiring layer over the substrate, interconnect wire being absent from the wiring layers over the second regions; and

fabricating a capacitor with metal-based charge-storage electrodes that extends through the first wiring layer and the portion of the second wiring layer over the second regions.

18. The process of claim 17, wherein the fabricated capacitor is a charge storage device for one of the DRAM cells.

19. The process of claim 17, wherein the DRAM cell includes a metal-oxide-semiconductor transistor, and the fabricating a capacitor couples one of the charge-storage electrodes to one of a drain and a source of the transistor.

20. The process of claim 17, wherein the fabricating a capacitor further comprises:
opening a window through more than the first and portion of the second wiring layers;
depositing material for one of the charge-storage electrodes on the window;
depositing a dielectric layer on the one of the charge-storage electrodes; and
depositing material for another of the charge-storage electrodes on the dielectric layer.

21. The process of claim 20, further comprising:
removing the deposited material for one of the charge-storage electrodes to form a gap between an outer surface of the wiring layer farthest from the substrate and the charge-storage electrode from which the deposited material was removed.

22. The process of claim 17, further comprising:
forming another wiring layer over the capacitor, one of interconnect wire and a metal plug in the another wiring layer making contact with one of the charge-storage electrodes.

23. The process of claim 17, wherein the fabricating a first wiring layer makes the layer with a copper-based dual damascene process.

24. The process of claim 17, wherein the fabricating makes two wiring layers.